Quality assurance testing of the ATLAS Tile-Calorimeter Phase-II upgrade low-voltage power supplies

R Mckenzie[1], E Nkadimeng[1], R Van Rensburg[1], T Lepota[1], N Njara[1] and B Mellado[1,2]

[1]University of the Witwatersrand, School of Physics and Institute for Collider Particle Physics, Johannesburg, South Africa
[2] iThemba LABS, National Research Foundation, PO Box 722, Somerset West 7129, South Africa

E-mail: ryan.peter.mckenzie@cern.ch

Abstract. The TileCal is a sampling calorimeter that forms the central region of the hadronic calorimeter of the ATLAS experiment. This detector is to undergo its Phase-II upgrade during Long-Shutdown 3, in the years from 2025 to mid-2027, in preparation for the start of operation of the HL-LHC. The TileCal phase-II upgrade consists of numerous elements such as the LVPSs which reside on-detector. A total of 256 LVPSs provide the TileCal on-detector electronics with +10 V DC power. An individual LVPS consist of a metalic box which contains an Embedded Local Monitoring Board attached to a motherboard, a fuse board, and eight transformer-coupled buck converters (Bricks) which are mounted to a cooling plate. Access to the Bricks is limited to only once per year due to their location within the inner-barrel. If a Brick experiences a failure it can be offline for up to a year resulting in the front-end electronics that it services being offline for this extended period as well. Therefore, the reliability of the Bricks is a key concern that needs to be addressed during their production. South Africa has committed to the production of 1024 Bricks which constitutes half of all the Bricks required. In order to ensure the reliability of these Bricks, once installed on-detector, quality assurance testing is implemented. These proceedings will provide an overview of the TileCal Phase-II upgrade, the motivation, and application for quality assurance testing of the Bricks, the development of the required apparatus as well as preliminary results.

1. Introduction

The TileCal is a sampling calorimeter that forms the central section of the Hadronic calorimeter of the ATLAS experiment [1]. It performs several critical functions within ATLAS such as the measurement and reconstruction of hadrons, jets, hadronic decays of τ-leptons and missing transverse energy. It also contributes to muon identification and provides inputs to the Level 1 calorimeter trigger system.

The detector is located in the pseudorapidity region $|\eta| < 1.7$ [1] and is partitioned into in a central barrel, known as Long Barrel, which is itself partitioned into two barrel regions (LBA and LBC). Two Extended Barrels (EBA and EBC) are located on either side of the Long Barrel. Each

[1] The pseudorapidity (η) is defined in terms of the polar angle θ as $\eta = -ln \tan(\theta/2)$.

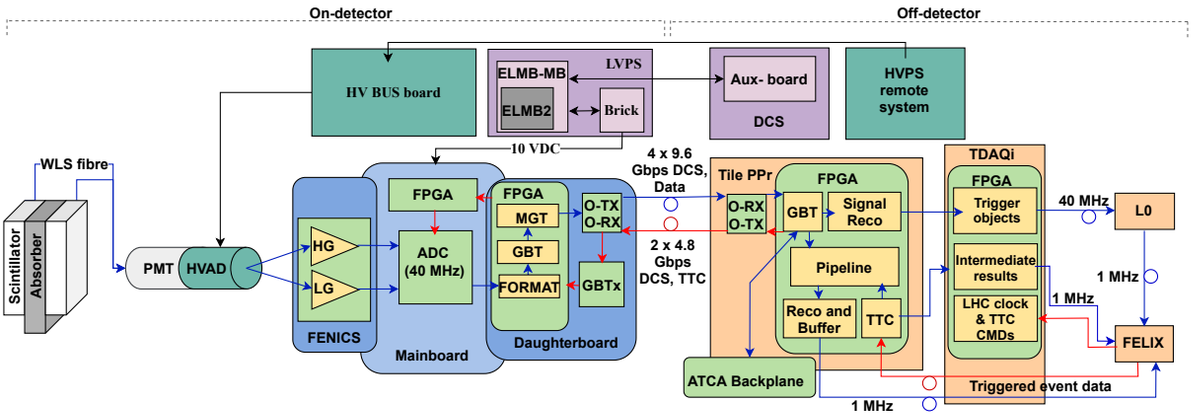

Figure 1. The HL-LHC Upgrade TileCal readout chain and power distribution system.

barrel region consists of 64 wedge shaped modules which cover an azimuthal angle of $\triangle\phi \sim 0.1$ and are composed of plastic scintillator tiles functioning as the active media inter-spaced by steel absorber plates.

In the third quarter of 2027 the start of the operation of the HL-LHC is planned with a foreseen peak luminosity of $5 \times 10^{34}\,\mathrm{cm}^{-2}\ \mathrm{s}^{-1}$. The resulting environment has necessitated the development of new electronics, both on- and off-detector, to ensure the continued peak performance of the detector under high pileup conditions and increased radiation exposure. The development of these electronic components falls under the ATLAS TileCal Phase-II upgrade.

2. The TileCal Phase-II upgrade

In order to meet the requirements of the HL-LHC a completely new read-out architecture will be implemented within TileCal, as illustrated in figure 1. In the new trigger and data acquisition architecture the output signals of the Tile detector cells will be digitized by the on-detector front-end electronics and then transferred off-detector for every bunch crossing for further processing [2].

The on-detector electronics and Photo-Multiplier Tubes (PMTs) of a module will be housed within a new drawer configuration. This configuration consists of a three-meter long drawer, known as Super-Drawer (SD), which slides into a girder on the outer radius of a module. Each SD is itself composed of either 4 or 3 independent Mini-Drawers (MD) depending on whether they are located in the barrel or extended barrel regions, respectively. The extended barrel makes use of 2 smaller drawers (Micro-drawers) in addition to 3 MDs resulting in both the barrel and extender barrel SDs being of the same length. The Micro drawers are un-instrumented and can contain up to 4 PMTS. The PMTs, located within the SDs of a module, are responsible for converting scintillation light into analog electrical signals which are then sent to the next stage of the signal chain. Most cells are read out by two PMTs, accounting for 9856 read-out channels in total and corresponding to 5182 cells. A total of 768 PMTs, which are located in the most exposed regions, will be replaced due to aging. A High-Voltage Active Divider (HVAD) is located at the end of every PMT, the function of which is to divide the input high voltage amongst the PMT dynodes utilizing active components thereby improving the linearity of their response. Located atop and attached to every HVAD is a Front End board for the New Infrastructure with Calibration and signal Shaping (FENICS). A FENICS is a readout electronics board that is responsible for the amplification and shaping of the analog signals received from a PMT. The two main roles of a FENICS are to read the fast signals using two gains and to read the average

current using six gains. A FENICS also contains two calibration systems, namely the charge injector system utilized for physics signal readout calibration, and the current injection system for the integrator readout. A Main Board (MB) is located within each MD of the TileCal. A single MB interfaces with twelve FENICS and one Daughter Board (DB). A MB digitizes the low- and high-gain signals received from the FENICS, which are then sent to its associated DB. The DBs are the primary interface between the on- and off-detector electronics and are mounted atop every MB. A DB transmits detector data to the off-detector electronics, receives and distributes the LHC clock, configurations, as well as slow-control commands. The High Voltage (HV) distribution system provides regulated HV power to the PMTs. It consists of off-detector HV Remote-boards that provide the primary HV, received from adjacent HV supply boards to the passive Bus-boards located within the MDs of all modules via 100m long cables. These Bus-boards then distribute the HV power to the HVADs. The three stage Low-Voltage (LV) system provides LV power to the Front-End electronics located within the SDs. The first stage of the LV system resides off-detector and is comprised of Auxiliary boards, that provide on/off control of the individual Bricks within a Low Voltage Power Supply (LVPS), as well as 200 V DC power supplies. A LVPS, of which one is located on the end of every SD, is comprised of eight transformer-coupled buck converters (Bricks) that function to step down the 200 V DC, received from the off-detector power supplies to 10 V DC. The 10 V DC power is then routed to point-of-load regulators which perform the final stepping down to that required by the local circuitry within the SDs. There is also an Embedded Local Monitoring Board (ELMB), that digitizes the signals received from the Bricks which are then sent to the Detector Control System (DCS) [3].

3. The Low-voltage power supply Bricks

A Phase-II Brick, of which there will be a total of 2048 within TileCal, provides a nominal output current of 2.3 A. These Bricks are of an iterative design with the latest version being the V8.4.2. As we can observe in Figure 2, at the centre of its design is the LT1681 controller chip [4]. It is dual transistor forward synchronous controller from Linear Technologies that operates at a fundamental frequency of 300 kHz. The LT1681 output clock pulse width is controlled via two inputs, the first of which is a slow feedback path that monitors the feedback voltage with a bandwidth of approximately 1 kHz. The second input is a fast feedback path that monitors the current through the low-side transistor on the primary side. The output clock is sent to the FET drivers, which perform the switching on the primary side. The design utilizes synchronous switching, That is, both the high-side and low-side transistors turn on and conduct for the duration that the output clock is in the high state, and both are off when the clock is in the low state. When the FETs conduct, current flows through the primary windings of the transformer, which then transfers energy to the secondary windings. The buck converter is implemented on the secondary side of the transformer. The output side also contains an additional inductor-capacitor stage for the filtering of noise. Voltage feedback for controlling the output voltage is provided.

Table 1. V8.4.2 Brick protection circuitry trip parameters

Protection circuitry	Trip parameters
Over voltage protection	11.50 V - 12.00 V
Over current protection	10.24 A - 10.75 A
Over temperature protection	70 °C $\geq$

 ISBN: 978-0-620-97693-0

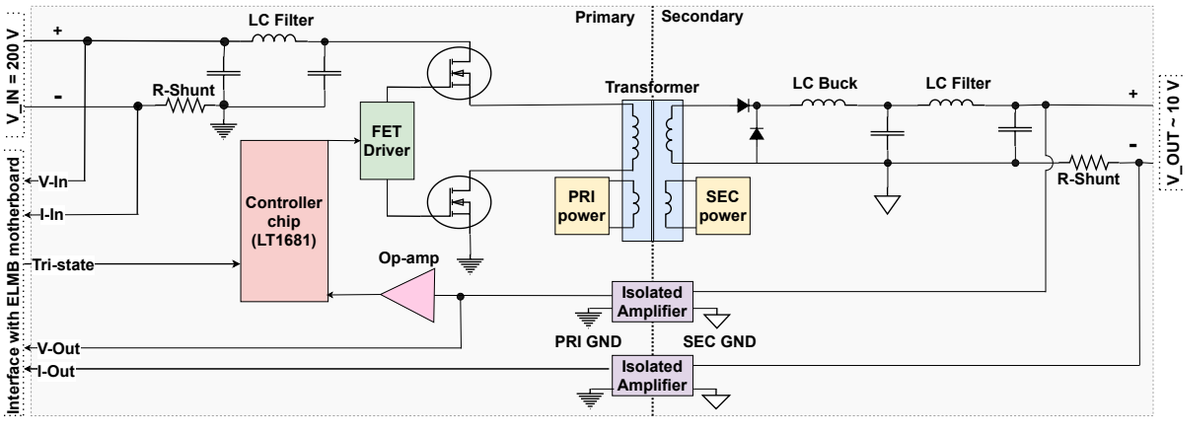

Figure 2. An updated functional block diagram of a Brick [2].

A Brick measures six analog signals and sends them to the ELMB motherboard, which include input voltage and current, output voltage and current, and the temperature readings from two points on the brick (primary and secondary side switches). In-built protection circuitry is also present in the Brick design in the form of over-voltage protection, over-current protection, and over-temperature protection. The purpose of this in-built protection is to initiate a trip if any of the trip criteria in Table 1 are met. This serves to limit damage to both the Brick as well as the electronics to which it provides power.

4. Quality assurance testing

Quality assurance testing plays a key role in the manufacturing process of electronics that require a high degree of reliability, as in the case of the Bricks. The emphasis placed on the reliability of the Bricks is due to their location within the inner-barrel of ATLAS which results in limited access on the order of once per year. Therefore a failed Brick and the electronics to which it provides power can be offline for up to a year. To prevent this outcome a quality assurance testing procedure illustrated in Figure 3 was developed. The procedure consists of four distinct steps namely the Visual inspection, Initial testing, Burn-in and Final testing steps.

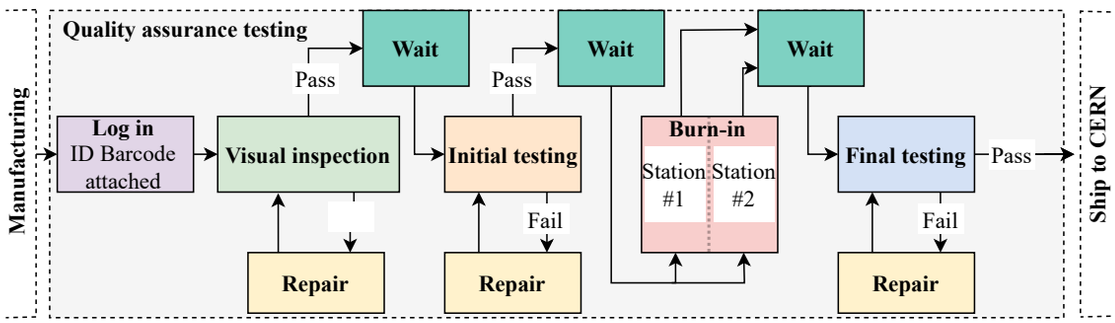

Figure 3. The quality assurance testing procedure for the Brick production.

4.1. Visual inspection

The Visual inspection step functions to detect macroscopic manufacturing defects. Automated visual inspection is undertaken at the assembly house. However, this inspection is performed

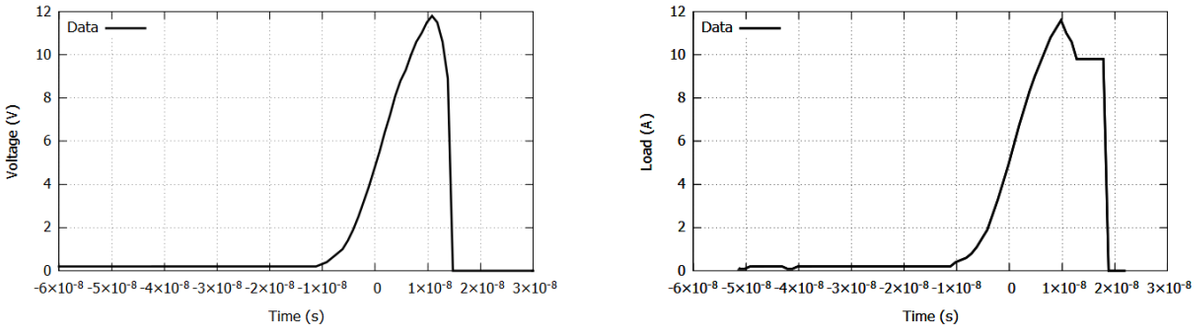

Figure 4. Brick over-voltage protection test data illustrating a pass (left). Brick over-current protection test data illustrating a failure (right). Data taken using a V8.4.2 Brick.

prior to the manual attachment of the thermal posts and the manual soldering of the transformer and connectors to the Bricks. Due to the this an additional visual inspection is undertaken by a Brick quality assurance expert upon arrival at the testing facility.

4.2. Initial/Final testing

Initial testing and Final testing make use of the same testing apparatus and procedure. They are differentiated by having occurred either before or after Burn-in testing, respectively. Both of these tests serve to ensure that the Bricks are operating within their design parameters by assessing various performance metrics. Examples of some of these metrics are the maximum startup delay, minimum output voltage, over-voltage trip point and over-current trip point. These tests are facilitated by the Initial/Final test station. The operating principle of this test station is to emulate the required input and output stages that a Brick requires for operation while piggybacking off of the Bricks inbuilt analogue monitoring hardware to monitor its performance. The input stage consists of a 200 V DC power supply which provides the input power for the Brick to step-down as well a low-voltage power supply which is used to send the Brick enable signal to power it on via a custom Interface board. The Interface board is also used to interface between the Brick and a National Instruments data-acquisition card for the transfer of the analog data to a PC for display and recording on a custom LabVIEW control program. The output stage consists of a dummy-load which converts the stepped down power received from the Brick into heat to be dissipated. An oscilloscope is used to measure the output clock frequency of the LT1681 controller chip by attaching a probe to a via which is itself connected to the output clock pin. The Initial/Final test station is fully operational with preliminary testing having occurred. In Figure 1, we can observe two of the multiple tests undertaken during the automated testing procedure. These are the over-voltage trip point and over-current trip point tests which make use of the parameters stated in Table 1. We can observe that the Brick tested passed the over-voltage trip point test with a trip having been initiated at 11.6 V. This as opposed to the over-current trip point test which was failed with a trip only having been initiated at 11.6 A. An undesirable latency period at 9.8 A can also observed.

4.3. Burn-in testing

Burn-in testing is an active means by which the reliability of the Bricks can be increased once installed on-detector. It is a form of accelerated aging which is used to address the high failure rate experienced by electronics during their early life as can be seen in Figure 5. Failures experienced in this region are known as infant mortality failures. These failures occur due to unavoidable manufacturing inconsistencies at both the device and component levels.

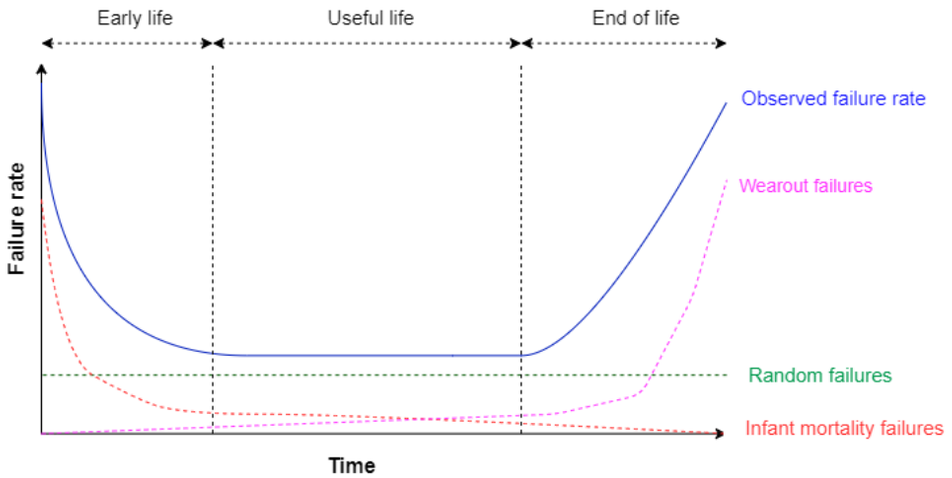

Figure 5. A generalized Bathtub-curve illustrating the failure rate as a function of time as experienced by electronic components.

Burn-in testing is used to artificially age the Bricks towards the useful life region, in which a lower constant failure rate is experienced before they are installed within the TileCal. By causing Bricks that would fail prematurely within the TileCal to rather fail during Burn-in testing increases the reliability of the Brick population once installed on-detector. This is achieved by subjecting the Bricks to a Burn-in cycle within a custom Burn-in apparatus in which they experience sub-optimal operating conditions which function to stimulate failure mechanisms within the Bricks. A Burn-in cycle consists of an 8-hour endurance run of the Bricks at a load of 5 A and an operating temperature of around 60° C which is twice the expected nominal on-detector operating temperature..

A custom Burn-in test station has been developed to undertake the Burn-in of eight Bricks per cycle. The station consists of a Main-board which multiplexes with the eight Brick-interface boards and the two Dummy-load boards as well as allowing for serial communication with the custom control and monitoring LabVIEW software.

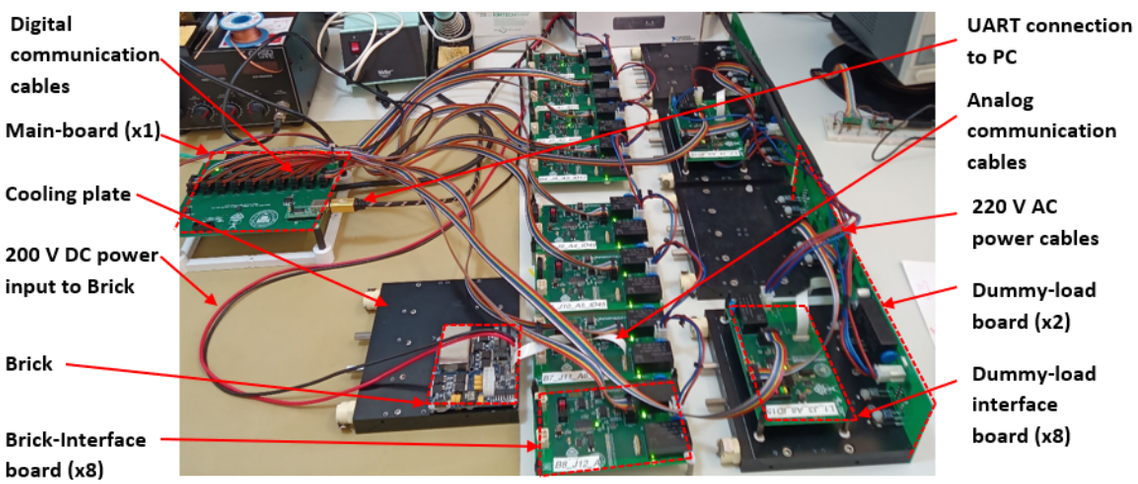

Figure 6. Calibration and fault finding of a Burn-in stations electronics before final integration with the chassis and cooling system.

A Brick-interface board provides the on/off control of a Brick and an analog to digital converter for the conversion of the analog data received from the Bricks measurements hardware. The custom Dummy-load boards provide a programmable load to be placed on the Bricks. The heat generated by the Dummy-load boards as well as the Bricks, due to power conversion inefficiency, is extracted by means of water cooled plates. An external DC input power supply for the Bricks as well as a water chiller form part of the test station.

5. Conclusions

The Contribution of South Africa to the TileCal Phase-II upgrade was described, with the quality assurance testing of Bricks to be produced being emphasized. The Bricks in-built protection circuitry was provided. Motivation for quality assurance testing of the Bricks was provided with the distinct Visual inspection, Initial testing, Burn-in testing and Final testing steps having been covered in detail. The custom testing apparatus was described and preliminary Initial testing data was presented an explained.

References

[1] The ATLAS Experiment at the CERN Large Hadron Collider (ATLAS Collaboration) 2008 *JINST* **3** S08003. 437 p also published by CERN Geneva in 2010 URL `https://cds.cern.ch/record/1129811`

[2] The ATLAS Tile-Calorimeter (ATLAS Collaboration) 2017 *published by CERN Geneva* **3** pg 87 – pg 156 URL `https://cds.cern.ch/record/2285583`

[3] R Mckenzie (ATLAS Collaboration) 2021 *published by CERN Geneva* URL `https://cds.cern.ch/record/2778343?ln=en`

[4] Analog Devices 2021 URL `https://www.analog.com/media/en/technical-documentation/data-sheets/1681f.pdf`